

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-181113

(43)Date of publication of application : 12.07.1996

(51)Int.Cl.

H01L 21/3065

C23C 16/50

C23F 4/00

H01L 21/68

H05H 1/46

(21)Application number : 06-320895

(71)Applicant : NISSIN ELECTRIC CO LTD

(22)Date of filing : 22.12.1994

(72)Inventor : MATSUDA KOJI

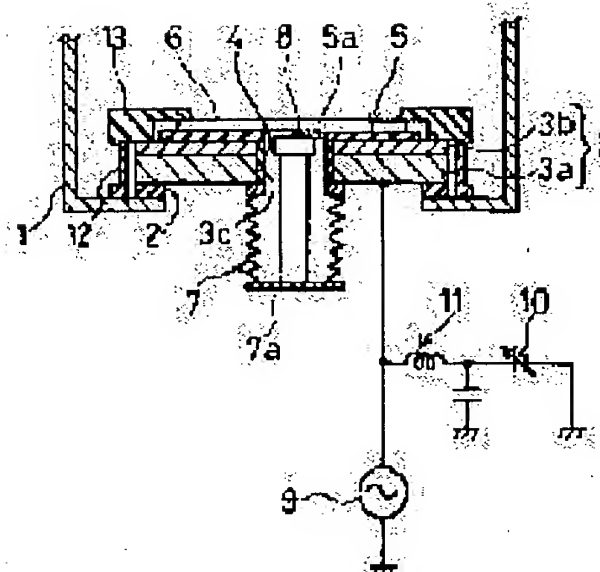
SASAMURA YOSHITAKA

## (54) PLASMA PROCESSOR

### (57)Abstract:

PURPOSE: To avoid the deterioration in an insulating film due to contact with plasma without covering the exposed part around a wafer on the insulating film with a covering member.

CONSTITUTION: A wafer presser for pressing a wafer 6 is provided as a covering member on an upper end surface of an auxiliary electrode 3b. In such a constitution, the exposed part of an insulating film 5 from the wafer 6 is covered with a wafer presser 13 so as not to be directly exposed to the insulating film 5 even if a chamber 1 is filled up with the plasma. Thus, the deterioration in the insulating film 5 by plasma can be avoided. Besides, the production of particles due to the contact of the insulating film 5 to the plasma can be avoided, then the replacement frequency of the insulating film 5 can be cut down since the deterioration in the film 5 can be avoided. Furthermore, the production of particles can be suppressed down to the level not to pose the ordinary plasma processing step.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

\* NOTICES \*

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

CLAIMS

---

[Claim(s)]

[Claim 1] While processing a wafer of a minor diameter with plasma generated when given to high-frequency power by the electrode from an insulator layer laid on an electrode through an insulator layer While carrying out adsorption maintenance on the above-mentioned electrode in electrostatic force generated by impressing direct current voltage to electrostatic force and the above-mentioned electrode which were generated on auto-bias voltage produced to the above-mentioned wafer according to plasma generating Plasma treatment equipment characterized by being covered with a covering member which a portion exposed to the perimeter of the above-mentioned wafer in the edge section and the above-mentioned insulator layer of the above-mentioned wafer becomes from an insulating material.

---

[Translation done.]

## \* NOTICES \*

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

DETAILED DESCRIPTION

---

## [Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to an etching system, a CVD system, and the other plasma treatment equipments that process a wafer using the plasma.

[0002]

[Description of the Prior Art] Plasma treatment equipments, such as RIE (Reactive Ion Etching) equipment, have processing effectiveness since a chemical reaction is quickly advanced by processing a sample using the plasma, and high processing quality, and it is fields, such as semiconductor fabrication machines and equipment, and is already established industrially.

[0003] For example, a plasma etching system etches a wafer 23 by the plasma which generated the etching gas with which it filled up in the chamber 21 by carrying out glow discharge by RF generator 22, as shown in drawing 4. The wafer 23 is laid through the insulator layer 26 on the lower electrode 25 of 2 block construction fixed through the insulating spacer 24 in the chamber 21. In this plasma etching system, electrostatic force is generated with the auto-bias voltage of the wafer 23 produced with generating of the plasma, and the direct current voltage impressed to the lower electrode 25 from DC power supply 27, and adsorption maintenance of the wafer 23 is carried out on the lower electrode 25.

[0004]

[Problem(s) to be Solved by the Invention] However, with the above-mentioned configuration, since it is formed so that an insulator layer 26 may usually serve as a larger path than a wafer 23, the portion exposed from the wafer 23 of an insulator layer 26 will be put to the direct plasma. For this reason, an insulator layer 26 will deteriorate, particle will occur and the inside of a chamber 21 will be polluted. Moreover, since an insulator layer 26 becomes easy to deteriorate in this way, the exchange frequency of an insulator layer 26 becomes high, and there is also un-arranging [ of causing the rise of a running cost ].

[0005] This invention is made in view of the above-mentioned situation, and aims at preventing deterioration of an insulator layer by adopting structure by which an insulator layer is not put to the direct plasma.

[0006]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, while plasma treatment equipment of this invention processes a wafer of a minor diameter with plasma generated when given to high-frequency power by the electrode from an insulator layer laid on an electrode through an insulator layer While carrying out adsorption maintenance on the above-mentioned electrode in electrostatic force generated by impressing direct current voltage to electrostatic force and the above-mentioned electrode which were generated on auto-bias voltage produced to the above-mentioned wafer according to plasma generating It is characterized by being covered with a covering member which a portion exposed to the perimeter of the above-mentioned wafer in the edge section and the above-mentioned insulator layer of the above-mentioned wafer becomes from an insulating material.

[0007]

[Function] With the above-mentioned configuration, since the portion exposed to the perimeter of a wafer on an insulator layer is covered with the covering member, it is lost that the above-mentioned portion is put to the direct plasma. So, deterioration of the insulator layer by touching the plasma can be prevented, and generating of the particle by film deterioration can be abolished.

[0008]

[Example] It will be as follows if one example of this invention is explained based on drawing 1 thru/or drawing 3 :

[0009] The plasma etching system concerning this example is equipped with the chamber 1 as a processing room, as shown in drawing 1 . This chamber 1 is filled with the etching gas introduced from a gas inlet (not shown) while vacuum length is made by the vacuum pump (not shown). This chamber 1 has the function as an anode, and is grounded.

[0010] On the opening periphery in the inferior-surface-of-tongue wall of a chamber 1, the lower electrode 3 which serves as a cathode through the insulating spacer 2 is arranged. The lower electrode 3 as an electrode consists of fixed electrode 3a currently fixed on the insulating spacer 2, and auxiliary-electrode 3b attached on fixed electrode 3a. Hole 3c penetrated up and down is formed in the center section of the lower electrode 3, and the inner skin is covered by the cylinder-like insulating material 4.

[0011] The insulator layer 5 of a path smaller than auxiliary-electrode 3b is formed in the upper limit side of auxiliary-electrode 3b. This insulator layer 5 has hole 5a almost equal to the bore of an insulating material 4 in the center section, and a wafer 6 is laid in an upper limit side. Auxiliary-electrode 3b is fixed with screws to fixed electrode 3a, and since it is removable, it can use the thing of a configuration according to the size of a wafer 6.

[0012] The bellows 7 expanded and contracted in the vertical direction is attached in the perimeter of a opening of hole 3c in the lower limit side of fixed electrode 3a. While bellows 7 is formed so that the interior may be airtight to atmospheric air like the inside of a chamber 1, base section 7a drives it in the vertical direction by the air cylinder (not shown) through an insulating material (not shown). Moreover, on base section 7a, the pedestal 8 which makes the conveyance location by the conveyance arm (not shown) go up and down a wafer 6 is being fixed.

[0013] While RF generator 9 is connected through a matching network (not shown), this RF generator 9 and DC power supply 10 prepared in juxtaposition are connected to fixed electrode 3a. Moreover, between DC power supply 10 and fixed electrode 3a, the LC circuit 11 is formed in order to measure inhibition of the RF from RF generator 9, and the bias voltage of a wafer 6.

[0014] The periphery edge of the lower electrode 3 and a predetermined gap (1mm - about 2mm) are set in the upper limit side of the base wall in a chamber 1, and the dark space shield 12 is being fixed to it. This dark space shield 12 is formed in order to prevent the abnormality discharge produced around the lower electrode 3, while fixing electrostatic capacity by the side of the lower electrode 3.

[0015] Moreover, on the upper limit side of auxiliary-electrode 3b, the wafer presser foot 13 which presses down a wafer 6 is formed as a covering member. As it is formed by insulating materials, such as polyimide system resin, and is shown in drawing 2 , from the periphery edge of a wafer 6, this wafer presser foot 13 is the range of width of face d (1mm - 2mm), is stuck inside also including orientation flat section 6a, and is pressed down. Moreover, the wafer presser foot 13 is formed so that the insulator layer 5 exposed without being covered with a wafer 6 may also be covered.

[0016] Although the above-mentioned wafer presser foot 13 is not illustrated to drawing 1 , it is driven by the elevator style as shown in drawing 3 . This elevator style is equipped with the rod 14 which pushes up the wafer presser foot 13 up, and is pulled down caudad, the bellows 15 which makes it go up and down a rod 14, and the air cylinder 16 which drives bellows 15. The above-mentioned rod 14 has penetrated the inferior-surface-of-tongue wall of a chamber 1, and it is supported so that there may not be axial Bure by the sleeve 17 insulating in the penetration portion. Bellows 15 is the thing of the same structure as the aforementioned bellows 7, and keeps the airtight condition the same.

[0017] With this plasma treatment equipment, the perimeter of the lower electrode 3 is made to go up and down the wafer presser foot 13 for the above elevator styles one piece or by having some, and rise and fall by the pedestal 8 of a wafer 6 are barred. In addition, in drawing 3 , the dark space shield 12 is

excluded for convenience.

[0018] In the above-mentioned configuration, if high-frequency power is given to the lower electrode 3 by RF generator 9 in case etching processing is performed, into the chamber 1 with which etching gas was filled, the plasma will be generated by glow discharge and etching processing of the wafer 6 will be carried out by this plasma. At this time, auto-bias voltage arises to a wafer 6 according to generating of the plasma. Moreover, direct current voltage is impressed to the lower electrode 3 by DC power supply 10 with grant of high-frequency power. Then, the electrostatic force generated with this direct current voltage and the electrostatic force generated with the above-mentioned auto-bias voltage act collectively, and adsorption maintenance of the wafer 6 is carried out on the lower electrode 3.

[0019] With the above configurations, since the portion exposed from the wafer 6 of an insulator layer 5 is covered with the wafer presser foot 13 even if the inside of a chamber 1 is filled with the plasma, an insulator layer 5 is not directly put to the plasma. So, deterioration of the insulator layer 5 by the plasma can be prevented, and generating of the particle by an insulator layer 5 touching the plasma can also be prevented. Moreover, since the function to hold a wafer 6 is also equipped with the wafer presser foot 13, immobilization of a wafer 6 becomes more certain.

[0020] As mentioned above, since deterioration of an insulator layer 5 can be prevented, it becomes possible to also reduce the exchange frequency of an insulator layer 5. Although the insulator layer 5 was specifically exchanged whenever it performed about 100 plasma treatment of a wafer 6 conventionally, according to this plasma etching system, plasma treatment was able to be performed, without exchanging to 1000 sheets. Moreover, it was stopped by the degree from which generating of particle does not pose a problem by the usual plasma treatment, either.

[0021] In addition, although this example explained the case where this invention was applied to a plasma etching system, of course, the same configuration which used the wafer presser foot 13 also for plasma treatment equipments, such as a CVD system, is applicable.

[0022]

[Effect of the Invention] While the plasma treatment equipment of this invention processes the wafer of a minor diameter with the plasma generated when given to high-frequency power by the electrode as mentioned above from the insulator layer laid on the electrode through the insulator layer While carrying out adsorption maintenance on the above-mentioned electrode in the electrostatic force generated by impressing direct current voltage to the electrostatic force and the above-mentioned electrode which were generated on the auto-bias voltage produced to the above-mentioned wafer according to plasma generating It is the configuration covered with the covering member which the portion exposed to the perimeter of the above-mentioned wafer in the edge section and the above-mentioned insulator layer of the above-mentioned wafer becomes from an insulating material.

[0023] The portion exposed to the perimeter of a wafer on an insulator layer is covered with a covering member by this, and it is lost that the above-mentioned portion is put to the direct plasma. So, deterioration of the insulator layer by touching the plasma can be prevented, and generating of the particle by film deterioration can be abolished.

[0024] Therefore, by adopting this plasma treatment equipment, the exchange frequency of an insulator layer can be reduced sharply and the effect that reduction of a running cost can be aimed at is done so.

---

[Translation done.]